What is claimed is:

[Claim 1] A control circuit, for an LCD device having a power module, a host control unit, and an image display unit, the power module supplying a plurality of potential levels for the LCD device, the control unit controlling a plurality of gate driving signals and a plurality of source driving signals for the image display unit, the control circuit comprising:

a signal delay unit, coupled to the image display unit; and
a signal detecting unit, coupled to the host control unit, wherein the signal detecting unit detects an on/off status of the LCD device from the host control unit, provides a disable signal to the power module, such that the voltage potential levels are disabled except a pixel transistor turning-on level, a plurality of pixel transistors of the image display unit are discharged via sources of the pixel transistors, and provides an all-gate-on signal to the signal delay unit, the all-gate-on signal is delayed for a first delay time by the signal delay unit and outputs to the image display unit.

[Claim 2] The control circuit as recited in claim 1, wherein the first delay time is before the pixel transistor turning-on level is reduced to a gate threshold voltage, and the second delay time is after an analog voltage source of the LCD device is reduced to a ground level.

[Claim 3] The control circuit as recited in claim 1, wherein the host control unit, the signal-detecting unit, and the signal delay unit are integrated into an Applied Specific Integrated Circuit (ASIC).

[Claim 4] A method of discharging pixel transistors of an LCD device, comprising:

detecting whether the LCD device stops displaying an image;
providing a first signal to disable a power module of the LCD device and turn off a pixel transistor turn-on potential level after a first delay time; and
providing a second signal to turn on all the pixel transistors after a second delay time.

[Claim 5] The method as recited in claim 4, further comprising:

assigning a start point of an all-gate-on period of all the pixel transistor after an analog voltage source supplying the LCD device is reduced to a ground voltage level, such that the pixel transistors are discharged via sources thereof within the first delay time; and
assigning an end point of the all-gate-on period of all the pixel transistor before the pixel transistor turn-on level reaches to a threshold voltage for turning on the pixel transistors.

[Claim 6] The method as recited in claim 4, wherein the pixel transistors are fabricated by utilizing Thin Film Transistor (TFT) technology.

[Claim 7] An Applied Specific Integrated Circuit (ASIC), for a capacitor charging/discharging device, having a plurality of capacitors, comprising:

a host control unit;
a signal detecting unit, receiving a first disable signal outputted from the host control unit and outputting a second disable signal to a power supply module outside of the ASIC, for disabling a part of the power supply module simultaneously, and disabling other part of the power supply module which controls the capacitors after a first delay time; and
a delay unit, receiving a second signal from the signal detecting unit, and outputting to the capacitor charging/discharging device after having paused for a second delay time, such that a plurality of switches controlling the capacitors are turned on.

[Claim 8] An LCD panel system, for operating an LCD panel controlled by at least a plurality of source driving signals and a plurality of gate driving signals, comprising:

a control circuit, outputting a plurality of data and a plurality of control signals;
a pixel array, coupled to the control circuit, having a plurality of pixels arranged in an array, wherein each of the pixels corresponds to a transistor for receiving at least one of the data provided from the control circuit and at least one of the control signals for displaying an image;

a power module, for supplying a plurality of potential levels to the LCD panel and receiving at least a part of the control signals from the control circuit, wherein when the control circuit detects the LCD panel has stopped to display the image, a first signal and a second signal are transmitted, wherein the first signal disables the power module and turns off a pixel transistor turn-on level after a first delay time, and the second signal turns on gates of the transistors corresponding to all of the pixels after a second delay time.

[Claim 9] The system as recited in claim 8, wherein the transistors are fabricated using film-forming technology of a Thin Film Transistor (TFT).

[Claim 10] The system as recited in claim 8, wherein the step of turning off the pixel transistor turn-on level after the first delay time comprises using a first delay device.

[Claim 11] The system as recited in claim 8, wherein the step of turning on the gates of the transistors of all the pixels after the second delay time comprises using a second delay device.

[Claim 12] The system as recited in claim 8, wherein the first signal indicating all potential levels supplied by the power module except the pixel transistor turn-on level to be turned off.

[Claim 13] The system as recited in claim 8, wherein the first signal and the second signal are low level enable signals.

[Claim 14] The system as recited in claim 8, wherein the host control unit, the signal detecting unit and the delay unit are integrated in an Applied Specific Integrated Circuit (ASIC).